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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/655,024	09/05/2003	Gun-Ok Jung	2557-000170/US	6042

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EXAMINER	
COX, CASSANDRA F	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/655,024	JUNG ET AL.	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-13* is/are allowed.

6)☒ Claim(s) *1,3,8 and 14* is/are rejected.

7)☒ Claim(s) *2,4-7 and 15-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/05/03, 07/02/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 15 is objected to because of the following informalities: In line 3 of claim 15 "second" should be replaced with --delayed--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 3 recites the limitation "the plurality of bit signals" in line 10 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 8, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takada et al. (U.S. Patent No. 5,955,902) in view of Ho et al. (U.S. Patent No. 6,426,660).

In reference to claim 1, Takada discloses in Figure 1 a frequency multiplier comprising a delay circuit (31) that receives a first clock signal (Fref) having a first

frequency and outputs a delayed clock signal (Fdel), the delay circuit (31) producing the delayed clock signal (Fdel) by applying a time delay to the first clock signal (Fref); a control circuit (32, 33) that detects a phase difference between the first clock signal (Fref) and the delayed clock signal (Fdel), and outputs a control signal (Vcont) to the delay circuit (31) corresponding to the detected phase difference, wherein the control signal controls a duration of the time delay applied to the first clock signal (Fref) by the delay circuit (31). Takada does not disclose the XOR gate. Ho discloses in Figure 3 an XOR gate (32) that receives the first clock signal (INPUT CLOCK) and the delayed clock signal (output of delay block 30), and outputs the second clock signal (OUTPUT CLOCK). It would have been obvious to tone skilled in the art at the time of the invention that the XOR gate (32) of Ho could be used to replace the multiplying circuit (38) of Takada (wherein the XOR gate 32 would receive the first clock signal (Fref/F1) and the delayed clock signal Fdel) for the advantage of being able to generate a second clock signal (OUTPUT CLOCK) having a 50% duty cycle. The same applies to claim 14.

In reference to claim 8, Ho discloses that the second clock signal (OUTPUT CLOCK) would have a second frequency that is twice that of the first frequency (INPUT CLOCK).

Allowable Subject Matter

7. Claims 9-13 are allowed.

8. Claims 2, 4-7, and 15-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claim 3 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: Claims 2, 6-7, 15, and 20 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the control signal (CTRL) includes a plurality of bit signals corresponding to the detected phase difference, each bit signal having a logic state in combination with the rest of the limitations of the base claims and any intervening claims. Claims 3-5 and 16-19 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the control circuit includes a comparator (232) and a counter (233) in combination with the rest of the limitations of the base claims and any intervening claims.

11. The following is an examiner's statement of reasons for allowance: Claims 9-13 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the control circuit includes a comparator (232) and a counter (233) in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:30 PM and on alternate Fridays from 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

CC
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August 4, 2004